AF/2133

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
DAWEI HUANG
FENG QI

Serial No.: 10/090,371

Filed: MARCH 4, 2002

For: ERROR CORRECTION TRELLIS CODING WITH PERIODICALLY INSERTED KNOWN SYMBOLS

Examiner: J. TORRES

Group Art Unit: 2133

Att'y Docket: 2100.003700

Customer No. 023720

APPEAL BRIEF

CERTIFICATE OF MAILING
37 C.F.R. 1.8

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Commissioner of Patents
P.O. Box 1450
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Sir:

Appellant hereby submits this Appeal Brief to the Board of Patent Appeals and Interferences in response to the final Office Action dated September 16, 2005. A Notice of Appeal was filed on December 1, 2005 and so this Appeal Brief is believed to be timely filed.

A check in the amount of $500.00 for filing this Appeal Brief is attached. However, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be required for any reason, the Assistant Commissioner is authorized to deduct said fees from **Williams, Morgan & Amerson's P.C. Deposit Account 50-0786/2100.003700.**

I. REAL PARTY IN INTEREST

The present application is owned by Lucent Technologies, Inc. The assignment of the present application to Lucent Technologies, Inc., is recorded at Reel 12672, Frame 0467.

II. RELATED APPEALS AND INTERFERENCES

Appellant is not aware of any related appeals and/or interferences that might affect the outcome of this proceeding.

III. STATUS OF THE CLAIMS

Claims 1-22 are pending in the application. Claims 17-22 stand rejected under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the enablement requirement. Claims 1-22 stand rejected under 35 USC 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter that Appellants regard as the invention and as allegedly being incomplete. Claims 10-22 stand rejected under 35 USC 101 because the claimed invention is allegedly directed to non-statutory subject matter. Claims 1-22 stand rejected under 35 U.S.C. § 102(b) as allegedly being obvious over Simanapalli (U.S. Patent No. 6,081,921) in view of Kato, et al (U.S. Patent No. 5,436,918).

IV. STATUS OF AMENDMENTS

There were no amendments after the final rejections.

V. SUMMARY OF CLAIMED SUBJECT MATTER

With regard to independent claims 1, 10, and 17, Appellants describe and claim, among other things, periodically inserting known symbols into a digital input data sequence and forming an expanded digital input data sequence based on a constraint length. For example, an encoder 14 may periodically insert a zero bit into an input data sequence after every (K-1) bits, where K is the constraint length associated with the encoder 14. See Patent Application, page 11, ll. 29-35. The constraint length of a convolutional encoder is defined in terms of the memory length and the code rate of the convolutional encoder. See Patent Application, page 13, ll. 13-16. For example, a constraint length may be determined, in part, by a length of a register that receives input from a receiving circuit. See Patent Application, page 11, ll. 13-16 and Figure 1. By periodically inserting known symbols into the digital input data sequence and forming the expanded digital input data sequence based on a constraint length, the present invention may reduce the computational complexity of the channel coding system, may reduce the required memory storages, and may reduce the bit error rate. See Patent Application, page 7, ll. 16-25.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Appellant respectfully requests that the Board review and overturn the four rejections present in this case. The following issues are presented on appeal in this case:

(A) Whether claims 17-22 fail to comply with the enablement requirement;

(B) Whether claims 1-22 are indefinite;

(C) Whether claims 10-22 are directed to non-statutory subject matter; and

(D) Whether claims 1-22 are obvious over Simanapalli (U.S. Patent No. 6,081,921) in view of Kato, et al (U.S. Patent No. 5,436,918).

VII. ARGUMENT

A. Legal Standards

The test of enablement is whether one reasonably skilled in the art could make or use the invention from the disclosures in the patent coupled with information known in the art without undue experimentation. *United States vs. Telectronics, Inc.*, 857 F.2d 778, 785 8 USPQ2d 1217, 1223 (Fed. Cir. 1998). A patent need not teach, and preferably omits, what is well known in the art. *In re Buchner*, 929 F.2d 660, 661, 18 USPQ2d 1331, 1332 (Fed. Cir. 1991).

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. That is, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Healthcare Corp.*, 110 F.3d 1573 (Fed. Cir. 1997). The mere fact that the prior art can be combined or modified does not make the resultant combination obvious unless the prior art also suggests the desirability of the

combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. Third, there must be a reasonable expectation of success.

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Appellant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. A recent Federal Circuit case emphasizes that, in an obviousness situation, the prior art must disclose each and every element of the claimed invention, and that any motivation to combine or modify the prior art must be based upon a suggestion in the prior art. *In re Lee*, 61 U.S.P.Q.2d 143 (Fed. Cir. 2002). Conclusory statements regarding common knowledge and common sense are insufficient to support a finding of obviousness. *Id.* at 1434-35. Moreover, it is the claimed invention, as a whole, that must be considered for purposes of determining obviousness. A mere selection of various bits and pieces of the claimed invention from various sources of prior art does not render a claimed invention obvious, unless there is a suggestion or motivation in the prior art for the claimed invention, when considered as a whole.

It is by now well established that teaching away by the prior art constitutes *prima facie* evidence that the claimed invention is not obvious. *See, inter alia, In re Fine,* 5 U.S.P.Q.2d (BNA) 1596, 1599 (Fed. Cir. 1988); *In re Nielson*, 2 U.S.P.Q.2d (BNA) 1525, 1528 (Fed. Cir. 1987); *In re Hedges*, 228 U.S.P.Q. (BNA) 685, 687 (Fed. Cir. 1986).

B. Claims 17-22 comply with the enablement requirement.

In the Final Office Action, the Examiner alleged that the specification does not state that the inserted zeroes comprise an equivalent time varying convolution code. Appellants respectfully disagree and note that the Patent Application describes a "zero code" comprising an

equivalent time varying convolutional code at least in lines 13-16 on page 10 of the specification and in lines 1-5 on page 13 of the specification. The specification also describes inserting the zero code, contrary to the Examiner's allegations. See Patent Application, page 13, ll. 20-25. Thus, Appellants respectfully submit that one reasonably skilled in the art could make or use the claimed invention from the disclosures in the patent application coupled with information known in the art without undue experimentation.

Appellants respectfully submit that the specification complies with the enablement requirement and request that the Examiner's rejections of claims 17-22 under 35 U.S.C. § 112, first paragraph, be REVERSED.

C. Claims 1-22 are definite.

In the Final Office Action, the Examiner alleges that "forming an expanded digital input data sequence based on a constraint length" is indefinite since it is not clear how the constraint length is used to form the expanded digital input data sequence. Appellants respectfully disagree and note that inserting zeros expands the digital input data sequence. Furthermore, one embodiment of the present invention inserts one zero after each (K-1) information bits, where K is the constraint length. See Patent Application, page 12, ll. 11-12. Accordingly, Appellants respectfully submit that the specification does describe forming an expanded digital input data sequence based on a constraint length.

In response to this argument, the Examiner alleges that a constraint length could be "almost any communication parameter that serves to constrain the communication system to a particular mode of operation." Appellants respectfully disagree and note that the constraint length of a convolutional encoder is defined in terms of the memory length and the code rate of

the convolutional encoder. See Patent Application, page 13, ll. 13-16. Appellants therefore submit that the Examiner has adopted an improperly broad interpretation of the term "constraint length" that conflicts with the definition presented in the specification and the definition that would be applied by a person of ordinary skill in the art.

Second, the Examiner alleges that the specification does not state that the inserted zeroes comprise an equivalent time varying convolution code. Appellants respectfully disagree and note that the Patent Application describes a "zero code" comprising an equivalent time varying convolutional code at least in lines 13-16 on page 10 of the specification and in lines 1-5 on page 13 of the specification. Appellants further submit that a person of ordinary skill in the art having benefit of the present disclosure will appreciate that the zero code comprises one or more zeros.

For at least the aforementioned reasons, Appellants respectfully submit that claims 1-22 are definite and request that the Examiner's rejections of claims 1-22 under 35 U.S.C. § 112, second paragraph, be REVERSED.

D. Claims 10-22 are directed to statutory subject matter.

In the Final Office Action, the Examiner alleges that computer programs are non-statutory. Appellants respectfully disagree and note that a computer program is statutory material if it produces a "useful, concrete and tangible result." See MPEP §2106. Appellants respectfully submit that the method set forth in independent claims 10 and 17 produces a useful, concrete and tangible result. In particular, the methods set forth in claims 10 and 17 produce a channel coded data stream. Furthermore, Appellants believe that the methods set forth in claims 10 and 17 fall under the safe harbor provided for processes that require measurements of physical objects or activities to be transformed outside of the computer into computer data. See MPEP §2106. In

particular, claims 10 and 17 set forth receiving a digital input data sequence that may be representative of a physical activity performed outside of the computer. For example, the digital input data sequence may be representative of an acoustic signal provided to a microphone.

In response to this argument, the Examiner alleges that the claims are directed to non-statutory subject matter because two Examiners could, in principle, carry out the method using a pencil and paper. Appellants respectfully submit that whether or not the claimed invention could, in principle, be carried out by hand is irrelevant to determining whether or not the claims are directed to statutory subject matter. As stated above, the criterion for determining whether or not a method constitutes statutory subject matter is whether or not the method produces a "useful, concrete and tangible result." See MPEP §2106.

For at least the aforementioned reasons, Appellants respectfully submit that claims 10-22 are directed to statutory subject matter and request that the Examiner's rejections of claims 10-22 under 35 USC 101 be REVERSED.

E. Claims 1-22 are not obvious over Simanapalli in view of Kato.

Simanapalli describes a convolutional encoder 22 that includes a bit insertion controller 28 which may interleave zero bits with input frame bits in an alternating manner. See Simanapalli, col. 3, ll. 3-18 and Figure 2. The Examiner alleges that inserting zero bits in an alternating manner is equivalent to forming an expanded digital input data sequence based on a constraint length of two. The Examiner also alleges that a constraint length could be "almost any communication parameter that serves to constrain the communication system to a particular mode of operation." Appellants respectfully disagree and submit that the Examiner has adopted an improperly broad interpretation of the term "constraint length" that conflicts with the

definition presented in the specification and the definition that would be applied by a person of ordinary skill in the art.

As defined in the specification and in accordance with common usage in the art, the constraint length of a convolutional encoder is defined in terms of the memory length and the code rate of the convolutional encoder. See Patent Application, page 13, ll. 13-16. For example, a constraint length may be determined, in part, by a length of a register that receives input from a receiving circuit. See Patent Application, page 11, ll. 13-16 and Figure 1. Appellants further note that Simanpalli has also defined the constraint length N in a manner consistent with the definition set forth in the present application and presented one conventional example in which the constraint length appears to be six. See Simanapalli, Figure 1 and related discussion. Thus, contrary to the Examiner's allegations, a constraint length cannot be "almost any communication parameter that serves to constrain the communication system to a particular mode of operation." In particular, simply inserting zero bits in an alternating manner, as described in Simanapalli, is not equivalent to forming an expanded digital input data sequence based on a constraint length of two. Accordingly, Appellants respectfully submit that Simanapalli fails to teach or suggest forming an expanded input data sequence based on a constraint length, *e.g.*, the constraint length of the convolutional encoder 22.

The Examiner relies upon Kato to describe reducing a number of connections between trellis nodes in a trellis by inserting fixed bits in a bit stream. The fixed bits may be inserted near the central portion of encoding information bit data. In the case of inserting a plurality of bits, the bits may be inserted concentratedly or distributively. See Kato, col. 4, ll. 7-16 and Figures 5A-B. However, Kato is also completely silent with regard to a constraint length. Accordingly,

Kato does not describe or suggest periodically inserting known symbols into a digital input data sequence and forming an expanded digital input data sequence based on a constraint length.

The cited references also fail provide any suggestion or motivation to modify the prior art to arrive at Appellants claimed invention. To the contrary, both of the cited references teach away from the Examiner's proposed modification of the prior art. Simanapalli appears to teach away from forming an expanded digital input data sequence based on a constraint length. In particular, Simanapalli describes interleaving zero bits with input frame bits in an alternating manner, *e.g.*, inserting a zero bit after every input bit. However, the convolutional encoder described in Simanapalli appears to have a constraint length of six. See Simanapalli, Figure 1 and related discussion. Kato also teaches away from the present invention. In particular, Kato teaches that fixed bits are inserted in a data stream to reduce a residual bit error ratio for the *same* line bit error ratio, whereas the present invention teaches periodically inserting known symbols to *reduce* the line bit error ratio. It is by now well established that teaching away by the prior art constitutes *prima facie* evidence that the claimed invention is not obvious.

For at least the aforementioned reasons, Appellants respectfully submit that the present invention is not obvious over Simanapalli in view of Kato and request that the Examiner's rejections of claims 1-22 under 35 U.S.C. 103(a) be REVERSED.

VIII. CLAIMS APPENDIX

The claims that are the subject of the present appeal – claims 1-22 – are set forth in the attached "Claims Appendix."

IX. EVIDENCE APPENDIX

There is no separate Evidence Appendix for this appeal.

X. RELATED PROCEEDINGS APPENDIX

There is no Related Proceedings Appendix for this appeal.

XI. CONCLUSION

In view of the foregoing, it is respectfully submitted that the Examiner erred in not allowing all claims pending in the present application, claims 1-22, over the prior art of record. The undersigned may be contacted at (713) 934-4052 with respect to any questions, comments or suggestions relating to this appeal.

Respectfully submitted,

Date: 2/1/06

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AGENT FOR APPELLANTS

CLAIMS APPENDIX

1. (Previously Presented) A system for channel coding data within a digital communications system comprising:

a data receiving circuit for receiving a digital input data sequence and periodically inserting known symbols into the digital input data sequence and forming an expanded digital input data sequence based on a constraint length; and

an encoder operatively connected to said data receiving circuit for trellis encoding the expanded digital input data sequence to produce a channel coded data stream such that the number of connections between trellis nodes in a trellis are reduced, said encoder operative according to the constraint length.

2. (Original) A system according to Claim 1, wherein the known symbols that are inserted comprise zeros.

3. (Original) A system according to Claim 2, wherein the inserted zeros comprise an equivalent time varying convolutional code.

4. (Original) A system according to Claim 1, wherein said encoder comprises a convolutional encoder

5. (Original) A system according to Claim 1, wherein the encoder applies code words that are one-to-one mappings of the distinct paths on a trellis to binary sequences.

6. (Original) A system according to Claim 1, wherein the topology of the trellis corresponds to memory length *m*, and the known symbols are inserted after each *m* symbol within the input data sequence.

7. (Original) A system according to Claim 1, wherein the encoder is operative as a generator matrix having a constraint length k=m-1, wherein m corresponds to the memory length, and the code rate is R=1/1 such that the known symbols are inserted after each k-1 information bit.

8. (Original) A system according to Claim 1, and further comprising a Maximum Likelihood (ML) decoder for receiving and decoding the channel coded data stream.

9. (Original) A system according to Claim 8, wherein the Maximum Likelihood (ML) decoder comprises a Viterbi decoder.

10. (Previously Presented) A method of channel coding data in a digital communications system comprising the steps of :

receiving a digital input data sequence;

periodically inserting known symbols into the digital input data sequence and forming an expanded digital input data sequence based on a constraint length; and

trellis encoding the expanded digital input data sequence based on the constraint length to produce a channel coded data stream such that the number of connections between trellis nodes in a trellis are reduced.

11. (Original) A method according to Claim 10, wherein the step of inserting known symbols comprises the step of inserting zeros into the digital input data sequence.

12. (Original) A method according to Claim 11, wherein the inserted zeros comprise an equivalent time varying convolutional code.

13. (Original) A method according to Claim 10, and further comprising the step of applying code words that are one-to-one mappings of the distinct paths on a trellis to binary sequences.

14. (Original) A method according to Claim 10, wherein the topology of the trellis corresponds to the memory length m, and further comprising the step of inserting a known symbol after each m symbol within the input data sequence.

15. (Original) A method according to Claim 10, and further comprising the step of decoding channel coded data stream within a maximum likelihood (ML) decoder.

16. (Original) A method according to Claim 15, and further comprising the step of decoding the channel coded data stream within a Viterbi decoder.

17. (Previously Presented) A method of channel coding data in a digital communications system comprising the steps of:

receiving a digital input data sequence;

periodically inserting known symbols into the digital input data sequence and forming an expanded digital input data sequence based on a constraint length k=m-l, wherein m corresponds to a memory length and a code rate is R=1/l, such that the known symbols are inserted after each k-l information bit; and

trellis encoding the expanded digital input data sequence to produce a channel coded data stream, wherein the number of connections between trellis nodes in a trellis are reduced.

18. (Original) A method according to Claim 17, wherein the step of inserting known symbols comprises the step of inserting zeros into the digital input data sequence.

19. (Original) A method according to Claim 18, wherein the inserted zeros comprise an equivalent time varying convolutional code.

20. (Original) A method according to Claim 17, and further comprising the step of applying code words that are one-to-one mappings of the distinct paths on a trellis to binary sequences.

21. (Original) A method according to Claim 17, and further comprising the step of decoding channel coded data stream within a maximum likelihood (ML) decoder.

22. (Original) A method according to Claim 21, and further comprising the step of decoding the channel coded data stream within a Viterbi decoder.